## REMARKS

This is intended as a full and complete response to the Final Office Action dated July 29, 2003, having a shortened statutory period for response set to expire on October 29, 2003. Claims 15 - 22 remain pending in the application and are shown above. Claims 15 - 22 are rejected by the Examiner. Reconsideration of the rejected claims is requested for reasons presented below.

Claims 15-22 stand rejected under 35 USC § 103(a) as being unpatentable over the combination of *Endo, et al* '150 (U.S. Patent No. 4,532,150), Europe '440 (*Loboda, et al.*, EP 725,440), applicant's admitted prior art, and *Chiang, et al.* (U.S. Patent No. 5,817,572). The Examiner asserts that it would have been within the scope of one or ordinary skill in the art to combine the teachings of *Endo et al.* '150, Applicants' admitted prior art, and Europe '440 with *Chiang* to enable the formation of the structure of Figure 1. The Examiner further asserts that the purpose for each step in *Chiang* is not relevant contrary to the assertion by Applicants. Applicants respectfully respond to this rejection.

*Endo et al.* '150 discloses a process for depositing silicon carbide on a substrate. The substrate may be metallic, such as aluminum material. Europe '440 discloses depositing a silicon carbon barrier layer on a metal surface, between two metal layers to prevent interlayer diffusion, or between a metal and a dielectric material to prevent diffusion of the metal into the dielectric material and insulate layers of wiring.

Applicant discloses knowledge of the use of dual damascene structures having barrier layers, etch stop layers, and passivation layers as disclosed in page 3, lines 15-30, of the specification. Applicants disclose knowledge that prior art barrier layers, etch stop layers, and passivation layers have had high dielectric constants.

*Chiang* discloses single damascene formation of via and trench layers by a first patterned dielectric layer formed over the semiconductor substrate that has a first opening formed through the first dielectric layer and an etch stop layer. The first opening is filled with a metal and planarized to form a metal plug damascene structure. A second patterned dielectric layer is formed over the first dielectric layer and has a second opening over at least a portion of the conductive metal. The second opening is then filled with a metal barrier layer and metal fill material and planarized to form an

interconnect damascene structure. The process may then be repeated. The dielectric etch stop may be silicon carbide. Alternatively, the etch stop layer may be formed as the first dielectric layer of the interconnect damascene structure and a photoresist is used to define the interconnect channel.

The Examiner errs in asserting that Applicants have argued the patentability of claim 15 on grounds that *Chiang* includes a silicon carbide etch stop for a different purpose. Applicants have argued that *Chiang* deposits the silicon carbide layer in a different method, and that the combined references do not motivate the method as recited in claim 15.

The combination of *Endo et al.* '150, Applicants admitted prior art as indicated by the Examiner in the paper mailed March 20, 2002, and Europe '440, with *Chiang* does not teach, show, or suggest depositing a silicon carbide barrier layer on the substrate by a method comprising introducing an alkylsilane and a noble gas into a chamber, initiating a plasma in the chamber, and reacting the alkylsilane in the presence of the plasma to form silicon carbide, depositing a first dielectric layer on the silicon carbide barrier layer, depositing a silicon carbide etch stop having an etch selectivity ratio of at least about 40 to 1 on the first dielectric layer by a method comprising introducing an alkylsilane and a noble gas into a chamber, initiating a plasma in the chamber, and reacting the alkylsilane in the presence of the plasma to form silicon carbide, patterning the silicon carbide etch stop, depositing a second dielectric layer on the silicon carbide etch stop, etching the first dielectric layer and the second dielectric layer to form a feature definition, as recited in claim 15, and claims dependent thereon. Withdrawal of the rejection is respectfully requested.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the Final Office Action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this Final Office Action.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the methods as recited and claimed. Having addressed all issues set out in the Final Office Action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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